

amendments to the claims. A typographical error on page 7 of the specification has been corrected. The page now provides for a "feed through phenomenon." Claim 4 has been amended to provide that the "plurality of capacitors are connected," rather than the "capacitor is connected." Claim 4 has also been amended to depend from Claim 1, as Claim 3 has been canceled. Similarly, Claim 6 has been amended to depend from Claim 1, as Claim 5 has been canceled. Claim 7 has been amended to remove the redundant recitation of an element now included in amended Claim 1. Claim 10 has been amended to recite "analog to digital converters."

CLAIM REJECTIONS – 35 U.S.C. § 103

Claims 1 to 4, 8, 9, and 11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over the Potts et al. U.S. Patent No. 5,332,893 [hereinafter referred to as "Potts,"] in view of the International Reference No. 231,767 [hereinafter referred to as the "International Reference".] Claim 1 now includes the recitations of Claim 5, which is allowable, so the rejection as applied to amended Claim 1, and dependent Claims 2, 4, 8 and 9, is believed moot. Claim 11 has been amended to include the recitations of Claim 5. The rejection as applied to amended Claim 11 is traversed.

Potts discloses a layered imaging stack that can bear a latent photostatic image comprising only a single segmented electrode on one side of the stack, rather than plate electrodes on each side of the stack. Appropriate sizing of the segmented electrodes enables individual electrodes to serve at different times as either the ground reference formerly provided by the electrode on the other side of the stack, or the collector of charge carriers representing the latent photostatic image. The imaging stack may be used with different types of imaging systems, and in flat or cylindrical configurations.

The International Reference discloses a readout circuit with a low pass filter and an amplifier sharing a common resistor.

As the Examiner has noted, the cited references fail to disclose or suggest all of the recitations of amended Claim 11. In particular, they fail to disclose or suggest a charge amount detection circuit that shares a plurality of capacitors connected to each other in parallel. Accordingly, full allowance of amended Claim 11 is requested.

Claims 12 to 15 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Potts in view of the International Reference, and further in view of the Ando Japanese Patent No. 361070872A. Claims 12 to 15 depend, directly or indirectly, upon amended Claim 11. For the reasons advanced above with respect to Claim 11, these claims are also believed allowable, and such action is requested.

In view of the above discussion and amendments, it is respectfully submitted that the present application is in condition for allowance. Therefore, reconsideration and allowance are requested.

Applicants also enclose a marked-up version of the changes made to the claims by the current amendment.

Respectfully submitted,

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By: Timothy Carter Pledger
Timothy Carter Pledger
Reg. No. 29,424
Attorney for Applicants

Dike, Bronstein, Roberts & Cushman
Intellectual Property Practice Group of
Edwards & Angell, LLP
P.O. Box 9169
Boston, MA 02209-4280
(617) 517-5505

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Words to be added are indicated by underscore, while words to be deleted are indicated by ~~strikeover~~.

IN THE SPECIFICATION:

Please rewrite the paragraph beginning on page 7, line 11, as follows:

The following description briefly deals with a voltage reading method that is so called as a correlated double sampling (hereinafter referred to as CDS). If the circuit system shown in Figure 4 is perfect, the voltage that has been read during the period C must correctly correspond to the signal charge amount. In actual, however, during the period D after the resetting, the output voltage of the CSA 20 is not perfectly equal to the reference voltage GND, thereby causing the generation of an offset voltage. Such an offset voltage is generated due to (a) an offset or a flicker noise of the operational amplifier 20a and/or (b) a ~~field~~ feed through phenomenon occurred when the TFT (switching devices 18) and/or the reset switch 20c turn on and off. The field through phenomenon is essential to MOS switches. According to

IN THE CLAIMS:

Please amend Claims 1, 4, 6, 7, 10, and 11 as follows:

1. (Amended) A charge amount detection circuit, comprising:
a charge sensitive amplifier;
a low pass filter circuit provided so as to follow the charge sensitive amplifier; and
a voltage amplifier circuit provided so as to follow the low pass filter circuit,

wherein one part of circuit elements constituting the low pass filter circuit and one part of circuit elements constituting the voltage amplifier circuit are commonly used;

wherein the low pass filter circuit and the voltage amplifier circuit share a plurality of capacitors that are connected with each other in parallel; and

a switch for switching between a state in which at least one of the capacitors are inserted in the charge amount detection circuit and a state in which said at least one of the capacitors are not inserted.

4. (Amended) The charge amount detection circuit as set forth in claim 3 1,
wherein the voltage amplifier circuit includes an operational amplifier having an inverted input terminal to which the capacitor is connected, and

the low pass filter circuit includes a resistor and the plurality of capacitors are capacitor
that is connected in series with the resistor.

6. (Amended) The charge amount detection circuit as set forth in claim 1 5,
wherein an amplification of the voltage amplifier circuit is 1 when the state in which said at least one of the capacitors are not inserted is made by the switch.

7. (Amended) The charge amount detection circuit as set forth in claim 1,
~~wherein the low pass filter circuit and the voltage amplifier circuit share a plurality of capacitors that are connected with each other in parallel, and~~
a plurality of switches for respective switching between a state in which at least one of the capacitors are inserted in the charge amount detection circuit and a state in which said at least one of the capacitors are not inserted, numbers of the capacitors that are switched by the respective switches being different from each other.

10. (Amended) The charge amount detection circuit as set forth in claim 1, further comprising:

a sampling hold circuit for holding a signal charge amount outputted from the voltage amplifier circuit;

an analog to digital converter ~~converters~~ for analog to digital converting the signal charge that has held by the sampling hold circuit;

a multiplexer for assigning a plurality of input terminals to ~~one of~~ the analog to digital converter ~~converters~~; and

a data latch circuit for holding the signal charge that has been converted into a digital value.

11. (Amended) A two-dimensional image sensor having a charge amount detection circuit, said circuit comprising:

a charge sensitive amplifier;

a low pass filter circuit provided so as to follow the charge sensitive amplifier; and

a voltage amplifier circuit provided so as to follow the low pass filter circuit,

wherein one part of circuit elements constituting the low pass filter circuit and one part of circuit elements constituting the voltage amplifier circuit are commonly used;

wherein the low pass filter circuit and the voltage amplifier circuit share a plurality of capacitors that are connected with each other in parallel; and

a switch for switching between a state in which at least one of the capacitors are inserted in the charge amount detection circuit and a state in which said at least one of the capacitors are not inserted.